Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of fabricating an integrated circuit, the method comprising:

depositing an etch stop layer over a first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

depositing an insulating layer after the etch stop layer is deposited over the etch stop layer;

forming a barrier layer extending along lateral side walls and a bottom of a via aperture, the via aperture being configured to receive a via material that electrically connects the first conductive layer and a second conductive layer; and

depositing a copper alloy via material in the via aperture on the barrier layer to form a via, the copper alloy material including Zinc (Zn) or Silver (Ag) and at least one element for increasing grain size including Calcium (Ca) or Chromium (Cr), wherein the copper alloy via material completely fills the via aperture.

2. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes silver (Ag).

3. (Previously Presented) The method of claim 2, wherein the copper alloy via material includes Zinc (Zn).

4. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes one atomic percent or less of Zinc (Zn) or Silver (Ag).

5. (Cancelled)

6. (Previously Presented) The method of claim 1, wherein the copper alloy via material includes Chromium (Cr).

7. (Cancelled)

8. (Previously Presented) The method of claim 6, wherein the element with a characteristic for increasing grain size is one atomic percent or less of Chromium (Cr).

9. (Original) The method of claim 6, wherein the increased grain size is between 0.5 and 3 μm.

10. (Currently Amended) A method of using ternary copper alloy to obtain a low resistance and large grain size interconnect or via, the method comprising:

providing a first conductive layer over an integrated circuit substrate;

providing an etch stop layer over the first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

providing an insulating layer over the etch stop layer after the etch stop layer has been provided over the first conductive layer;

providing a conformal layer section extending along a bottom and sides of a via aperture positioned over the first conductive layer to form a barrier separating the via aperture from the first conductive layer;

filling the via aperture completely with a ternary copper alloy via material to form a ternary copper alloy via on the conformal layer, the ternary copper alloy including at least one element for lowering resistivity and at least one of Chromium (Cr) or Calcium (Ca), wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via; and

providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer to the second conductive layer.

11. (Previously Presented) The method of claim 10, wherein the ternary copper alloy via material is at least 98 atomic percent copper.

12. (Previously Presented) The method of claim 11, wherein the ternary copper alloy via includes Zinc (Zn), Silver (Ag), or Tin (Sn).

13. (Previously Presented) The method of claim 11, wherein the ternary copper alloy via includes one atomic percent or less of Chromium (Cr) or Calcium (Ca).

14. (Cancelled)

15. (Previously Presented) The method of claim 10, wherein the element with a characteristic for increasing grain size is Calcium (Ca) or Chromium (Cr).

16. (Previously Presented) The method of claim 10, wherein the element with a characteristic for increasing grain size is one atomic percent or less of the ternary copper alloy via material.

17. (Currently Amended) A method of forming a via in an integrated circuit, the method comprising:

depositing a first conductive layer;

depositing an etch stop layer over the first conductive layer, wherein the etch stop layer is in direct contact with the first conductive layer;

depositing an insulating layer over the etch stop layer;

forming an aperture in the insulating layer and the etch stop layer;

providing a barrier material extending along a bottom and sides of the aperture to form a barrier layer;

filling the aperture completely with a ternary copper alloy via material to form a ternary copper alloy via on the barrier material, the ternary copper alloy via including at least one of the following pairs of elements: Tin and Calcium; Tin and Chromium; Zinc and Chromium; Zinc and Calcium; Silver and Chromium; and Silver and Calcium, wherein the

ternary copper alloy via material includes an element with a characteristic for increasing grain size of the ternary copper alloy via; and

providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer and the second conductive layer.

18. (Previously Presented) The method of claim 17, wherein the ternary copper alloy via material includes copper (Cu), tin (Sn), and Calcium (Ca).

19. (Original) The method of claim 17, wherein the ternary copper alloy via material includes copper (Cu), zinc (Zn), and chromium (Cr).

20. (Previously Presented) The method of claim 17, wherein the ternary copper alloy is CuAgCr, or CuSnCa.

21. (Cancelled)

22. (Previously Presented) The method of claim 17, wherein the ternary copper alloy via includes stuffed grain boundaries.

23. (Original) The method of claim 17, wherein the grain size of the ternary copper alloy via is 0.5 to 3 μm.